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EXAMINER

PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 10/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/512,149

Applicant(s)

AGARWAL, VISHNU K

Examiner

Marcos D. Pizarro-Crespo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-14 and 56-89 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-14 and 56-89 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 30,34.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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Attorney's Docket Number: MI22-1322

Filing Date: 2/23/2000

Claimed Foreign Priority Date: none

Applicant(s): Agarwal

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 33 filed on 7/15/2003.

Continued Examination Under 37 CFR 1.114

1. A request for a continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after the final rejection in paper no. 29, filed on 3/12/2003. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/15/2003 has been entered.

Acknowledgment

2. The amendment in paper no. 33, filed on 7/15/2003, in response to the Office action in paper no. 29, mailed on 3/12/2003, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this office action are claims 1, 4-14, and 56-89.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

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4. Claims 71, 78, and 80 are rejected under 35 U.S.C 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. Claim 71 describes a trench within which a first electrode layer of a capacitor is formed. The description in the original disclosure fails to support this limitation in the claim. Although the specification (pp.12/II.24-pp.13/II.3) describes an opening within which a first capacitor electrode is formed, it fails to describe said opening as a trench.

6. Claim 78 describes a conductive region between the first capacitor electrode and the substrate, wherein the conductive region is made of a monolithic unitary material. The description in the original disclosure fails to support this limitation in the claim. The specification (pp.12/II.18-19) listed several materials from which to make the conductive region. A *monolithic unitary material*, however, is not listed in the specification.

7. Claim 80 describes a high-K dielectric crystalline material that is *less than* 80% crystalline. The description in the original disclosure fails to support this limitation in the claims. The specification (pp.7/II.16-17) discloses a high-K dielectric layer having a crystalline portion that may be 70% crystalline or greater. The open-ended numerical range in claim 80 specifying a portion of the dielectric layer to be 80% crystalline or less does not meet the description requirement because the phrase "less than" has 0% as its lower limit causing the claims to literally read on embodiments outside of the disclosed range.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

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The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 80 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 80 describes a *crystalline* material that is *less than* 80% crystalline. This open-ended percentage range has 0% as its lower limit. However, a layer that is 0% crystalline is *not* crystalline. This contradicts the limitations in the claim that purports to further describe the *crystalline* layer in claim 1.

11. The following is a quotation of the fourth paragraph of 35 U.S.C. 112:

Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed. A multiple dependent claim shall not serve as a basis for any other multiple dependent claim. A multiple dependent claim shall be construed to incorporate by reference all the limitations of the particular claim in relation to which it is being considered.

12. Claim 80 is rejected under 35 U.S.C. 112, fourth paragraph, as being improper dependent claims for failing to include every limitation of the claims from which they depend. Applicant is required to cancel or amend the claims to place the claims in proper dependent form, or to rewrite the claim(s) in independent form.

13. The limitations in claim 80 infringe the limitations in basic claim 1. Whereas claim 1 recites that the crystalline layer is 70-90% crystalline, claim 80 recites that the crystalline layer is *less than* 80% crystalline, *i.e.*, 0-80%. The range in claim 1 excludes some percentages from the range in claim 80. Specifically, the percentages below 70% are excluded in claim 1.

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Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claims 1, 4-11, 13, 14, 56, and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan (US 5192871) in view of Motorola (US 5943580).

16. Regarding claim 1, Ramakrishnan shows (see, e.g., fig. 2) most aspects of the instant invention including an integrated circuitry comprising a capacitor comprising:

- a first capacitor electrode **14**
- a second capacitor electrode **20**
- a high-K capacitor-dielectric region between the capacitor electrodes comprising:
 - a high-K substantially-amorphous-material layer **18**
 - a high-K substantially-crystalline-material layer **16** over the amorphous-material layer **18**

wherein the crystalline and the amorphous layers may be made out of different chemical compositions (see, e.g., col.2/ll.46-50).

Ramakrishnan, however, fails to disclose that the crystalline-material layer is 70-90% crystalline. Nonetheless, the degree of crystallinity (or amorphicity) of a dielectric layer is considered a parameter subject to optimization and it is not patentable unless unobvious or unexpected results are obtained from it.

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Motorola (see, e.g., col.3/ll.5-15), for example, teaches that by selecting the crystallinity percentage of dielectric layers one is able to create capacitors with a wide range of dielectric constants on a single substrate. In other words, controlling the degree of crystallinity of Ramakrishnan's dielectric layer gives the skilled artisan control over the dielectric constant of the capacitor dielectric.

Consequently, it would be an obvious matter of design choice for one of ordinary skill in the art at the time the invention was made to select the degree of crystallinity of Ramakrishnan's dielectric layer since this is a variable of importance subject to routine experimentation and optimization that, as taught by Motorola, will give control over the dielectric constant of the capacitor dielectric, and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235.

17. Regarding claim 4, Ramakrishnan shows at least one of the first and second electrodes comprising a metal (see, e.g., col.1/ll.60).

18. Regarding claims 5-9, 11, 13, and 14, Ramakrishnan's shows (see, e.g., fig. 2):

- the capacitor over a semiconductor substrate **12**
- the dielectric layer received between the first and second capacitor plates **14 20**
- the amorphous layer **18** contacting the first capacitor electrode **14**
- the crystalline layer **16** contacting the second capacitor electrode **20**
- the dielectric layer as the only capacitor dielectric region between the capacitor electrodes **14 20**

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- the amorphous material layer **18** received between the semiconductor substrate **12** and the crystalline dielectric layer **16**

19. Regarding claims 10, 56, and 80, see the comments stated above in paragraph 16 with respect to claim 1, which are considered repeated here.

20. Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan and Motorola, as applied to claims 1 and 11 above, and further in view of Graettinger (US 5844771).

21. Ramakrishnan/Motorola shows most aspects of the instant invention (see paragraphs 16-19 above), except for a capacitor wherein the semiconductor substrate comprises bulk monocrystalline silicon. Graettinger (see, e.g., col.1/ll.20-24) teaches that in the processing of integrated circuits the substrate typically comprises monocrystalline silicon.

It would have been obvious at the time of the invention to one of ordinary skill in the art to have the substrate of Ramakrishnan/Motorola comprising monocrystalline silicon, as suggested by Graettinger, because in the processing of integrated circuits the substrate is typically monocrystalline silicon.

22. Claims 57-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan/Motorola in view of Narui (US 6201728) and Merchant (US 6235594).

23. Ramakrishnan/Motorola shows most aspects of the instant invention (see paragraphs 16-19 above), except for an insulative layer between the substrate and the capacitor electrodes. Narui (see, e.g., col.7/ll.47-55), on the other hand, teaches that an insulating layer formed between the substrate and the capacitor insulates the electrodes

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thereof and hence the leakage current is minimized. Merchant further teaches that this insulation layer is typically silicon dioxide (see, e.g., col.2/ll.15-20, col.3/ll.61-col.4/ll.11).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time of the instant invention to include a silicon-dioxide insulative film between Ramakrishnan/Motorola's substrate and his capacitor, as suggested by Narui and Merchant, to minimize the leakage current.

24. Claims 60-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan/Motorola in view of Eguchi (US 5442585) and Shrivastava (US 5557122).

25. Ramakrishnan/Motorola shows most aspects of the instant invention (see paragraphs 16-19 above), except for the specific capacitor-dielectric thickness claimed by the applicants *i.e.*, an amorphous dielectric thickness of 20-250Å, a crystalline dielectric thickness of 20-90Å, and a capacitor-dielectric region of 40-500Å.

Ramakrishnan, however, shows that the crystalline-dielectric layer may have a thickness of 100Å (see, e.g., col.3/ll.44) and that the amorphous-dielectric layer should be as thin as possible in order to prevent degradation of the capacitor performance (see, e.g., col.4/ll.20-26). Although Ramakrishnan/Motorola does not specify the same thicknesses as those claimed by the applicants, thickness differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes.

Shrivastava, for example, teaches that the capacitor-dielectric thickness is a design variable that if reduced will increase the capacitance of the capacitor (see, e.g.,

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col.2/ll.59-63). Likewise, Eguchi teaches that in order to increase the capacitance of a capacitor, the thickness of the capacitor dielectric should be reduced; however, if the film is made too thin, the performance of the capacitor deteriorates (col.1/ll.44-48).

Accordingly, it would be an obvious matter of design choice to select a suitable thickness for the capacitor-dielectric layers of Ramakrishnan, as taught by Shrivastava and Eguchi, since the capacitor-dielectric thickness is a variable of importance subject to routine experimentation and optimization and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235. Furthermore, it appears that the thickness differences between Ramakrishnan/Motorola's dielectric layer and the one claimed produce no functional differences and therefore would have been obvious. Note *In re Leshin*, 125 USPQ 416.

26. Claim 81 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan/Motorola in view of Yanagita (US 6376332).

27. Ramakrishnan/Motorola shows most aspects of the instant invention (see paragraphs 16-19 above), except for the integrated circuitry formed over a semiconductor-on-insulative substrate. Yanagita (see, e.g., col.1/ll.25), on the other hand, teaches that doing so will increase the operating speed of the circuitry.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to form the integrated circuitry of Ramakrishnan/Motorola over a semiconductor-on-insulative substrate, as suggested by Yanagita, to increase the operating speed of the circuitry.

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28. Claims 63-66 and 73-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara (US 5561307) in view of Mueller (US 5864496) and Koh (US 5920775).

29. Mihara shows (see, e.g., figs. 11-20) most aspects of the instant invention including an integrated circuitry comprising:

- a substrate **62** having an upper surface
- at least two gate structures **42A** laterally spaced apart from one another and formed over the upper surface of the substrate **62**, the two gate structures **42A** having uppermost surfaces (see, e.g., fig. 11)
- insulative material **66** formed over the two gate structures **42A** and the upper surface of the substrate **62**
- an opening formed in the insulative material **66**
- a capacitor comprising (see, e.g., fig. 16):
 - a first electrode layer **91** formed within the opening with a portion most proximate to the upper surface of the substrate **66** being elevationally below the uppermost surface of the gate structures **42A** (see, e.g., fig. 16).

Note: Although not shown in figure 16, Mihara teaches (see, e.g., col.10/II.50-67) that a contact layer may be optionally formed between the first electrode layer and the substrate, thus, spacing the most proximate portion of the first electrode layer from the upper surface of the substrate. As shown in figures 9 and 14, in doing so the portion of the first electrode layer most proximate to the upper

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surface of the substrate is kept elevationally below the uppermost surface of the gate structures.

- a dielectric layer formed over the first electrode layer **91** and within the opening, wherein the dielectric layer comprises material **92** other than ferroelectric material
- a second electrode layer **97** formed over the dielectric layer

It should be noted that the section of the DRAM wafer shown in figure 11 of Mihara depicts two cells and a single word line to which the gate structures are electrically connected (see, e.g., Mihara/col.13/ll.7-23). As a consequence, the opening in figure 11 is not shown between two gate structures. Nonetheless, as is well known, there are hundreds of identical cells fabricated in a DRAM wafer (see, e.g., Mihara/col.1/ll.15-20). Accordingly, one of ordinary skill in the art would have expected the structure in figure 11 to repeat itself within the wafer (see, e.g., Mihara/col.1/ll.15-20). Mueller reinforces Mihara's teaching. See, for example, col.1/ll.21-32, where Mueller teaches that DRAM chips employ millions of memory cells arranged in a plurality of rows and columns. The plurality of word lines run parallel to each other with the memory-cell gates electrically connected to the word lines.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art that Mihara's opening should have been between at least two gate structures, as taught by Mueller, since employing a plurality of word lines running parallel to each other with gate structures electrically connected to the word lines is common knowledge in the art.

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In addition, Mihara teaches that the dielectric layer comprises a high-K dielectric material **96** and an insulating material **92**, which may be silicon dioxide or other insulating layer. Koh (see, e.g., col.8/ll.10-30), on the other hand, teaches that replacing the silicon dioxide with a high-K dielectric material will increase the performance of Mihara's capacitor.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to have high-K materials for the dielectric layer of Mihara, as suggested by Koh, to increase the performance of the capacitor.

30. Regarding claim 64, Mihara shows that the dielectric layer may have at least a portion comprising crystalline material (see, e.g., col.11/ll.8-13).

31. Regarding claim 65, Mihara shows that the dielectric layer may have at least a portion comprising amorphous material (see, e.g., col.11/ll.8-13).

32. Regarding claim 66, Mihara shows that the dielectric layer may comprise a portion of amorphous material and a portion of crystalline material (see, e.g., col.11/ll.8-13).

33. Regarding claim 73, Mihara shows (see, e.g., fig. 14) a conductive region **36** may be formed between the first electrode layer and the substrate, the conductive region **36** electrically connecting the first electrode layer and the substrate.

34. Regarding claim 74, Mihara teaches that the conductive region may comprise conductive polysilicon (see, e.g., col.12/ll.39).

35. Regarding claim 75, Mihara teaches that the conductive region may comprise a metal (see, e.g., col.12/ll.39).

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36. Regarding claim 76, Mihara (see, *e.g.*, col.10/ll.5-15,60 and col.12/ll.39) shows that the conductive region may comprise a metal compound and a conductive barrier layer material.

37. Regarding claim 77, Mihara teaches that the conductive region may comprise a material different from that of the first electrode (see, *e.g.*, col.9/ll.59 and col.12/ll.39).

38. Regarding claim 78, Mihara teaches that the first electrode layer may comprise a monolithic unitary material (see, *e.g.*, col.9/ll.59).

39. Regarding claim 79, Mihara teaches that the first electrode may comprise conductively doped polysilicon (see, *e.g.*, col.14/ll.3).

40. Claims 67 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara/Mueller in view of Ramakrishnan.

41. Regarding claims 67, Mihara/Mueller shows most aspects of the instant invention (see paragraphs 29-39 above), except for the dielectric layer comprising an amorphous layer adjacent to the first electrode layer and a crystalline layer adjacent to the second electrode layer. Ramakrishnan, on the other hand, teaches (see, *e.g.*, col.3/ll.23-29) that such a structure prevents migration of impurities into the dielectric layer.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to have the dielectric layer of Mihara/Mueller comprising an amorphous layer adjacent to the first electrode layer and a crystalline layer adjacent to the second electrode layer, as suggested by Ramakrishnan, to prevent the migration of impurities into the dielectric layer.

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42. Regarding claim 68, Mihara/Mueller shows most aspects of the instant invention (see paragraphs 29-39 above), except for the dielectric layer comprising a crystalline layer adjacent to the first electrode and an amorphous layer adjacent to the second electrode. Ramakrishnan (see, e.g., col.2/ll.43-50), on the other hand, teaches that such a structure prevent the migration of impurities that may otherwise alter the dielectric characteristics of the dielectric layer.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to have Mihara/Mueller's dielectric layer comprising a crystalline layer adjacent to the first electrode and an amorphous layer adjacent to the second electrode, as suggested by Ramakrishnan, to protect the dielectric characteristics of the dielectric layer.

43. Claims 63, 71-73, 75, 76, and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele (US 5760474) in view of Koh.

44. Schuele shows (see, e.g., fig. 6) all aspects of the instant invention including an integrated circuitry comprising:

- a substrate **30** having an upper surface
- at least two gate structures **34, 35** laterally spaced from one another and formed over the upper surface of the substrate **30**, the two gate structures **34, 35** having uppermost surfaces
- insulative material **37** formed over the two gate structures **34, 35** and the upper surface of the substrate **30**

- an opening **38** formed in the insulative material **37** between the two gate structures **34, 35**
- a capacitor comprising:
 - a first electrode layer **50** formed within the opening **38** and having a portion most proximate and spaced from the upper surface of the substrate **30**, the portion being elevationally below the uppermost surfaces of the two gate structures **34, 35**
 - a dielectric layer **60** formed over the first electrode layer **50** and within the opening **38**, wherein the dielectric layer may comprise material other than ferroelectric material (see, e.g., col.3/ll.4)
 - a second electrode layer **70** formed over the high-K dielectric layer **60**

Schuele, however, fails to specify that the dielectric layer comprises high-K material. Koh (see, e.g., col.8/ll.10-30), on the other hand, teaches that doing so will increase the performance of Schuele's capacitor.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to have high-K materials for the dielectric layer of Schuele, as suggested by Koh, to increase the performance of the capacitor.

45. Regarding claim 71, Schuele shows the opening is a trench (see, e.g., fig. 2).

46. Regarding claim 72, Schuele shows the second electrode layer **70** is formed within the opening **38** (see, e.g., fig. 4).

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47. Regarding claim 73, Schuele shows a conductive region **42** intermediate the first electrode layer **50** and the substrate **30**, the conductive region **42** electrically connecting the first electrode layer **50** and the substrate **30**.

48. Regarding claim 75, Schuele shows the conductive region **42** comprising a metal (see, e.g., col.4/ll.6-15).

49. Regarding claim 76, Schuele shows the conductive region **42** comprising a material different from that of the first electrode **50** (see, e.g., col.4/ll.6-15).

50. Regarding claim 78, Schuele shows the first electrode layer comprising a monolithic unitary material (see, e.g., col.5/ll.15).

51. Claims 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele/Koh in view of Ramakrishnan.

52. Regarding claims 64-66, Schuele/Koh shows most aspects of the instant invention (see paragraphs 44-50 above), except for at least a portion of the dielectric layer comprising crystalline material. Ramakrishnan, on the other hand, teaches (see, e.g., col.2/ll.36-40) that it is desirable to have a portion of Schuele/Koh's dielectric layer comprising crystalline material to achieve the highest dielectric constant possible. Ramakrishnan further teaches (see, e.g., col.2/ll.46-50,col.3/ll.23-29) that having a portion of the dielectric layer comprising an amorphous material will help to obviate the inclusion of foreign materials into the crystalline portion of the layer.

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to have Schuele/Koh's dielectric layer comprising crystalline material and another portion comprising amorphous material, as suggested by

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Ramakrishnan, to achieve the highest possible dielectric constant while at the same time obviating the inclusion of foreign materials into the crystalline portion of the layer.

53. Regarding claim 67, see the comments stated above in paragraph 55 with respect to claims 64-66, which are considered repeated here. In addition, Ramakrishnan shows (see, e.g., fig. 2) the amorphous layer **18** adjacent to the first electrode layer **14** and the crystalline layer **16** adjacent to the second electrode layer **20**.

54. Regarding claim 68, see the comments stated above in paragraph 55 with respect to claims 64-66, which are considered repeated here. In addition, Ramakrishnan shows (see, e.g., fig. 1) the crystalline layer **16** adjacent to the first electrode **14** and the amorphous layer **18** adjacent to the second electrode **20**.

55. Claims 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele/Koh in view of Motorola.

56. Regarding claim 69, Schuele/Koh shows most aspects of the instant invention (see paragraphs 44-50 above), except for the high-K dielectric layer comprising a crystalline portion that is 70-98% crystalline.

Motorola (see, e.g., col.3/ll.5-16), on the other hand, teaches that by selecting the crystallinity percentage of high-K dielectric layers one is able to create capacitors with a wide range of dielectric constants on a single substrate. In other words, controlling the degree of crystallinity of Schuele/Koh's dielectric layer provides control over the capacitor dielectric constant.

Consequently, it would be an obvious matter of design choice for one of ordinary skill in the art at the time the invention was made to select the degree of crystallinity of

Schuele/Koh's dielectric layer since this is a variable of importance subject to routine experimentation and optimization that, as taught by Motorola, will give control over the capacitor dielectric constant, and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235.

57. Regarding claim 70, Schuele/Koh shows most aspects of the instant invention (see paragraphs 44-50 above), except for the high-K dielectric layer comprising an amorphous portion that is 70-98% amorphous.

Motorola (see, e.g., col.3/ll.5-16), on the other hand, teaches that by selecting the amorphicity percentage of high-K dielectric layers one is able to create capacitors with a wide range of dielectric constants on a single substrate. In other words, controlling the degree of amorphicity of Schuele/Koh's dielectric layer gives control over the capacitor dielectric constant.

Consequently, it would be an obvious matter of design choice for one of ordinary skill in the art at the time the invention was made to select the degree of amorphicity of Schuele/Koh's dielectric layer since this is a variable of importance subject to routine experimentation and optimization that, as taught by Motorola, will give control over the capacitor dielectric constant, and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235.

58. Claim 82 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele/Koh in view of Yanagita (US 6376332).

59. Schuele/Koh shows most aspects of the instant invention (see paragraphs 44-50 above), except for the integrated circuitry formed over a semiconductor-on-insulative

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substrate. Yanagita (see, e.g., col.1/ll.25), on the other hand, teaches that doing so will increase the operating speed of the circuitry.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to form the integrated circuitry of Schuele/Koh over a semiconductor-on-insulative substrate, as suggested by Yanagita, to increase the operating speed of the circuitry.

Claim Rejections - 35 USC § 102

60. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

61. Claim 83 is rejected under 35 U.S.C. 102(b) as being anticipated by Mihara.

62. Regarding claim 83, Mihara shows (see, e.g., fig. 16) all aspects of the instant invention including an integrated circuitry comprising:

- a substrate **62** having insulative material **66** formed over the substrate **62**
- an opening formed in the insulative material **66**
- a capacitor comprising:
 - a first electrode layer **91** formed within the opening
 - a high-K dielectric layer **96** formed over the first electrode layer **91** and within the opening
 - a second electrode layer **97** formed over the high-K dielectric layer **96**

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wherein the high-K dielectric layer **96** may comprise a portion of amorphous material and a portion of crystalline material (see, e.g., col.11/ll.8-18).

63. Claims 84-86 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara in view of Motorola.

64. Regarding claims 84-86 and 88, Mihara shows most aspects of the instant invention (see paragraph 62 above). He, however, fails to disclose a specific degree of crystallinity (or amorphicity) for the crystalline portion and/or the amorphous portion of the dielectric layer. Nonetheless, the specific degrees of crystallinity (or amorphicity) of the dielectric layer claimed by the applicant are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from them.

Motorola (see, e.g., col.3/ll.5-15), for example, teaches that by selecting the crystallinity percentage of dielectric layers one is able to create capacitors with a wide range of dielectric constants on a single substrate. In other words, controlling the degree of crystallinity of Mihara's dielectric layer gives the skilled artisan control over the dielectric constant of the capacitor dielectric.

Consequently, it would be an obvious matter of design choice for one of ordinary skill in the art at the time the invention was made to select the degree of crystallinity (or amorphicity) of Mihara's dielectric layer since this is a variable of importance subject to routine experimentation and optimization that, as taught by Motorola, will give control over the dielectric constant of the capacitor dielectric, and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235.

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65. Claims 83, 87, and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele in view of Ramakrishnan.

66. Regarding claim 83, Schuele shows (see, e.g., fig. 6) most aspects of the instant invention including an integrated circuitry comprising:

- a substrate **30** having insulative material **37** formed over the substrate **30**
- an opening formed in the insulative material **37**
- a capacitor **75** comprising:
 - a first electrode layer **50** formed within the opening
 - an insulating layer **60** formed over the first electrode layer **50** and within the opening
 - a second electrode layer **70** formed over the insulating layer **60**

Schuele, however, fails to show that the insulating layer **60** is formed of a high-K material comprising a crystalline portion and an amorphous portion. Ramakrishnan, on the other hand, teaches it would be highly advantageous to Schuele's capacitor insulating layer to have a high-K dielectric material having a crystalline portion and an amorphous portion. This structure will provide the sought-after high-dielectric constant that characterizes crystalline capacitor dielectrics, while at the same time preventing the migration of foreign materials that may adversely affect the dielectric constant of the capacitor-insulating layer. See, e.g., Ramakrishnan, col.1/ll.45-50,col.2/ll.35-57, and col.3/ll.23-30.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to have a high-K dielectric material having a crystalline portion

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and an amorphous portion for the capacitor insulating layer of Schuele, as suggested by Ramakrishnan, to protect the dielectric properties of the layer.

67. Regarding claim 87, Ramakrishnan shows that the high-K dielectric layer may comprise Ta₂O₅ (see, e.g., col.3/ll.53).

68. Regarding claim 89, Ramakrishnan shows (see, e.g., col.2/ll.48) that the portion of amorphous material and may comprise a different material than that of the portion of crystalline material.

Response to Arguments

69. The applicant argues:

Motorola fails to provide any teachings about specific crystallinity ranges. No design choice or routine experimentation can be performed without some basic teachings about specific ranges on which to base the design choice and routine experimentation.

The examiner responds:

The prior art clearly teaches that the degree of crystallinity (or amorphicity) of a dielectric layer is a parameter subject to optimization and; therefore, it is not patentable unless unobvious or unexpected results are obtained from it. *In re Aller* 220 F.2d 454, 456, 105 USPQ 233, 235 CCPA 1955.

Motorola (see, e.g., col.3/ll.5-15), for example, teaches that by selecting the crystallinity percentage of dielectric layers one is able to create capacitors with a wide range of dielectric constants on a single substrate. In other words, controlling the degree of crystallinity of Ramakrishnan's dielectric layer provides the skilled artisan with the ability to control the dielectric constant of the capacitor dielectric.

Consequently, it would be an obvious matter of design choice for one of ordinary skill in the art at the time the invention was made to select the degree of crystallinity for

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a dielectric layer since this is a variable of importance subject to routine experimentation and optimization that, as taught by Motorola, will provide control over the dielectric constant of the capacitor dielectric, and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235.

70. Applicant's arguments with respect to claims 63-79 and 81-89 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

71. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **-7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

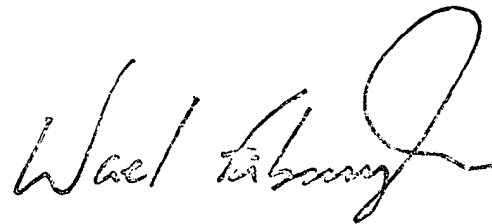
72. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 9:30 AM to 8:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

73. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

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74. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/310, 438/240, 361/313	9/23/2003
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	9/23/2003



SUPERVISORY PRIMARY EXAMINER
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